~~25~~. (Amended) The apparatus recited in claim [24] ~~23~~, wherein said first and said second processors comprise processors dedicated to control separate and independent functions in a system.

31. (Amended) An apparatus comprising a plurality of processors and a plurality of memories, each processor having write access at any time to only a particular one of said memories and read access at any time to any of said memories, wherein at least one of said processors in said plurality operates independently of other processors in said plurality.

REMARKS

Claims 23-34 were pending in the instant application. By way of the instant preliminary amendment, claims 24 and 33 have been canceled. Claims 23, 25-32, and 34 are now pending for consideration.

The rejection under 35 U.S.C. § 102(b) is no longer applicable as the features of claim 24 have been included in claim 23 and the features of claim 33 have been included in claim 31.

The rejection under 35 U.S.C. § 103 over Cutts and Nagai is respectfully traversed.

First, Cutts cannot be modified to have the processors to operate independent of each other, because it teaches a fault-tolerant configuration employing multiple identical CPUs executing the same instruction stream. A modification of Cutts with independently operating CPUs would destroy the functionality of Cutts. Therefore, the assertion that the combination of Cutts and Nagai would "increase system functionality (since there are two independent processors, each of them would perform different function)" is respectfully traversed.

Second, there would be no motivation to modify the circuit of Nagai to include the private write memory arrangement